

In the Claims:

Please cancel claims 26-50. Please amend claims 1-6 and 22. Please add new claims 51 and 52. The claims are as follows:

1. (CURRENTLY AMENDED) An electronic structure, comprising:

an internally circuitized substrate having a metallic plane on a first surface of the substrate; and

a redistribution structure having N dielectric layers denoted as dielectric layers 1, 2, ..., N, N metal planes denoted as metal planes 1, 2, ..., N, and a microvia structure through the N dielectric layers, wherein N is at least 2, wherein dielectric layer 1 is on the first surface of the substrate and on the metallic plane, wherein metal plane J is on dielectric layer J for J = 1, 2, ..., N, wherein dielectric layer I is on dielectric layer I-1 and on metal plane I-1 for I = 2, ..., N, and wherein the microvia structure electrically couples metal plane N to the metallic plane, wherein the microvia structure includes at least one microvia, and wherein each microvia of the at least one microvia is a blind via having an outer wall surface and an end surface with an electrically conductive plating on the outer wall surface and on the end surface such that the electrically conductive plating includes a continuous distribution of electrically conductive material on the outer wall surface along an entire perimeter of the blind via.

2. (CURRENTLY AMENDED) The electronic structure of claim 1, wherein the at least one microvia structure includes N microvias denoted as microvias 1, 2, ..., N, wherein the microvia K passes through dielectric layer K for K = 1, 2, ..., N, wherein metal plane N is electrically coupled to microvia N, wherein metal plane J-1 electrically couples microvia J to microvia J-1 for J = 2,

3, ..., N, and wherein microvia 1 is electrically coupled to the metallic plane.

3. (CURRENTLY AMENDED) The electronic structure of claim 1, wherein the at least one microvia structure includes a microvia that passes through the N dielectric layers, wherein the microvia electrically couples metal plane N to the metallic plane.

4. (CURRENTLY AMENDED) The electronic structure of claim 1, wherein the at least one microvia structure includes a first microvia, wherein the first microvia passes through dielectric layers M through N, wherein M is at least 2, wherein N is at least 3, wherein M is less than N, and wherein metal plane N is electrically coupled to the first microvia.

5. (CURRENTLY AMENDED) The electronic structure of claim 4, wherein the at least one microvia structure further includes a second microvia that passes through dielectric layers 1 through M-1, wherein metal plane M-1 electrically couples the first microvia to the second microvia, and wherein the second microvia is electrically coupled to the metallic plane.

6. (CURRENTLY AMENDED) The electronic structure of claim 4, wherein the at least one microvia structure further includes M-1 second microvias denoted as second microvias 1, 2, ..., M-1, and wherein the second microvia K passes through dielectric layer K for K = 1, 2, ..., M-1, wherein the metal plane M-1 electrically couples the first microvia to second microvia M-1, wherein if M > 2 then metal plane J-1 electrically couples second microvia J to second microvia J-1 for J = 2, 3, ..., M-1, and wherein second microvia 1 is electrically coupled to the metallic

plane.

7. (ORIGINAL) The electronic structure of claim 1, wherein N = 2 or N = 3.

8. (ORIGINAL) The electronic structure of claim 1, wherein the N dielectric layers each include a dielectric material having a stiffness of at least about 700,000 psi.

9. (ORIGINAL) The electronic structure of claim 1, wherein the N dielectric layers each include a dielectric material having a glass transition temperature of at least about 150 °C.

10. (ORIGINAL) The electronic structure of claim 1, wherein the N dielectric layers each include a dielectric material having a coefficient of thermal expansion of no more than about 50 ppm/°C.

11. (ORIGINAL) The electronic structure of claim 1, wherein at least one of the metallic plane and the N metal planes includes a signal plane.

12. (ORIGINAL) The electronic structure of claim 1, wherein at least one of the N metal planes includes a power plane.

13. (ORIGINAL) The electronic structure of claim 1, wherein at least one of the N metal planes includes a ground plane.

14. (ORIGINAL) The electronic structure of claim 1, wherein the substrate includes a dielectric material comprising a polytetrafluoroethylene (PTFE) having silicon particles therein.

15. (ORIGINAL) The electronic structure of claim 14, wherein the substrate further includes a ground plane, a power plane, and a signal plane, wherein the ground plane, the power plane, and the signal plane are each embedded within the dielectric material, and wherein the signal plane is disposed between the ground plane and the power plane.

16. (ORIGINAL) The electronic structure of claim 14, wherein the substrate further includes a ground plane, first and second power planes, and first and second signal planes, wherein the ground plane, the first and second power planes, and the first and second signal planes are each embedded within the dielectric material, wherein the first signal plane is disposed between the ground plane and the first power plane, and wherein the second signal plane is disposed between the ground plane and the second power plane.

17. (ORIGINAL) The electronic structure of claim 1, further comprising an electronic device electrically coupled to the metal plane N by a solder member.

18. (ORIGINAL) The electronic structure of claim 17, wherein the electronic device includes a semiconductor chip.

19. (PREVIOUSLY AMENDED) The electronic structure of claim 17, wherein the electronic

structure includes at least one power plane, and wherein a thickness of the redistribution structure is large enough that a nearest distance between the solder member and any power plane of the at least one power plane is not less than a predetermined minimum distance value.

20. (ORIGINAL) The electronic structure of claim 19, wherein the predetermined minimum distance value is predetermined by requirements of a given radio frequency application.

21. (ORIGINAL) The electronic structure of claim 1, wherein a plated through hole (PTH) passes through the substrate from the first surface to a second surface of the substrate, and wherein the metallic plane is electrically coupled to the PTH.

22. (CURRENTLY AMENDED) The electronic structure of claim 21, further comprising a second metallic plane on the second surface of the substrate and a second redistribution structure having P second dielectric layers denoted as second dielectric layers 1, 2, ..., P, P second metal planes denoted as second metal planes 1, 2, ..., P, and a second microvia structure through the P second dielectric layers, wherein P is at least 1, wherein second dielectric layer 1 is on the second surface of the substrate and on the second metallic plane, wherein second metal plane J is on second dielectric layer J for J = 1, 2, ..., P, wherein if I > 1 then second dielectric layer I is on second dielectric layer I-1 and on second metal plane I-1 for I = 2, ..., P, wherein the second microvia structure electrically couples the second metal plane P to the second metallic plane, and wherein the second metallic plane is electrically coupled to the PTH, wherein the second microvia structure includes one or more microvias, and wherein each microvia of the one or

more microvias is a blind via having an outer wall surface and an end surface with an electrically conductive plating on the outer wall surface and on the end surface such that the electrically conductive plating includes a continuous distribution of electrically conductive material on the outer wall surface along an entire perimeter of the blind via.

23. (ORIGINAL) The electronic structure of claim 22, wherein P = N.

24. (ORIGINAL.) The electronic structure of claim 22, further comprising an electronic board electrically coupled to the second metal plane N by a solder member.

25. (ORIGINAL.) The electronic structure of claim 24, wherein the electronic board includes a circuit card.

26-50. (CANCELED)

51. (NEW) The electronic structure of claim 1, wherein the electrically conductive plating on the outer surface of each blind via of the at least one microvia is a metal plating.

52. (NEW) The electronic structure of claim 51, wherein the electrically conductive material is copper.